EM78F734N

8-Bit Microcontroller

Product Specification

DOC. VERSION 1.2

ELAN MICROELECTRONICS CORP.

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Contents

Specification Revision History

Doc. Version	Revision Description	Date
1.0	Initial version	2014/05/13
1.1	1. Added Channel ADC6 to ADC 2. Added package SSOP20 3. Modified TC1CR, TC2DA and TC2DB description. 4. Modified SSOP16 package type. 5.Added SOP16 150mil package type.	2015/08/10
1.2	1. Add User Application Notice 2. Added Word 0 Bit 12 HLP description. 3. Added Appendix A “Ordering and Manufacturing Information”	2016/03/31

User Application Note

(Before using this chip, take a look at the following description note, it includes important messages.)

1. The internal TCC will stop running when in sleep mode. However, during AD conversion, when TCC is set to “SLEP” instruction, if the ADWE bit of the RE register is enabled, the TCC will keep on running.

2. During ADC conversion, do not perform output instruction to maintain precision for all of the pins. In order to obtain accurate values, it is necessary to avoid any data transition on I/O pins during AD conversion

3. The noise rejection function is turned off in the Fs and sleep mode

1 General Description

The EM78F734N is an 8-bit microprocessor designed and developed with low-power, high-speed CMOS technology and high noise immunity. It has an on-chip 4K×13-bit Electrical Flash Memory and 128×8-bit In-system programmable EEPROM. It provides three protection bits to prevent intrusion of user's Flash memory code.

With its enhanced Flash-ROM feature, the EM78F734N provides a convenient way of developing and verifying user's programs. Moreover, this Flash-ROM device offers the advantages of easy and effective program updates, using development and programming tools. Users can avail of the ELAN Writer to easily program their development codes.

2 Features

- **CPU Configuration**
  - 4K×13 bits Flash memory
  - 144×8 bits on-chip registers (SRAM)
  - 128 bytes In-system programmable EEPROM
  - 8-level stacks for subroutine nesting
- **I/O Port Configuration**
  - Three bidirectional I/O ports
  - Wake-up port : P6
  - 12 Programmable pull-down I/O pins
  - 8 programmable pull-high I/O pins
  - 4 programmable open-drain I/O pins
  - External interrupt : P60
- **Operating Voltage Range:**
  - 2.2V~5.5V @ – 40°C ~85°C (Industrial)
  - 2.2V~5.5V @ 0°C ~70°C (Commercial)
- **Operating frequency range (base on two clocks):**
  - IRC Drift Rate (Vdd @ 3.3V)

Internal RC Frequency	Drift Rate		
	Temperature (-10°C+40°C)	Process	Total
455kHz	±1%	±1%	±2%
1 MHz	±1%	±1%	±2%
4 MHz	±1%	±1%	±2%
8 MHz	±1%	±1%	±2%

  - IRC Drift Rate (Temperature: -10°C+40°C)

Internal RC Frequency	Drift Rate		
	Voltage (3.0~3.6V)	Process	Total
455kHz	±1%	±1%	±2%
1 MHz	±1%	±1%	±2%
4 MHz	±1%	±1%	±2%
8 MHz	±1%	±1%	±2%

- **One 16-bit Timer/Counter**
  - TC1 : Timer/Counter/Capture
- **One 8-bit Timer/Counter**
  - TC3 : Timer/Counter/PDO (Programmable Divider Output) / PWM (Pulse Width Modulation)
- **Eight available interrupts:**
  - Internal interrupt: 4
  - External interrupt: 4
- **Eight channels Analog-to-Digital Converter with 12-bit resolution**
- **Peripheral Configuration**
  - 8-bit real Timer Clock/Counter (TCC) with selective signal sources, trigger edges, and overflow interrupt
  - Power down (Sleep) mode
  - Four programmable Level Voltage Reset (LVR) (LVR) : 3.3V, 3.0V, 2.6V, and 2.0V (POR)
  - Three security registers to prevent intrusion of Flash memory codes
  - One configuration register to accommodate user's requirements
  - Two clocks per instruction cycle
  - High EFT immunity
  - Two sub-frequencies; 128kHz and 16kHz, the 16kHz is provided by dividing the 128kHz
- **Single instruction cycle commands**
- **Five Crystal Range in Oscillator Mode**

Crystal Range	Oscillator Mode
20 MHz ~ 12 MHz	HXT2
12 MHz~6 MHz	HXT1
6 MHz ~ 1 MHz	XT
1 MHz ~ 100kHz	LXT1

- **Programmable free running Watchdog Timer**
- **Package Type:**
  - 16-pin DIP 300mil : EM78F734ND16
  - 16-pin SOP 300mil : EM78F734NSO16
  - 16-pin SOP 150mil : EM78F734NSO16A
  - 16-pin SSOP 150mil : EM78F734NSS16
  - 18-pin DIP 300mil : EM78F734ND18
  - 18-pin SOP 300mil : EM78F734NSO18
  - 20-pin DIP 300 mil : EM78F734ND20
  - 20-pin SOP 300mil : EM78F734NSO20
  - 20-pin SSOP 209mil : EM78F734NSS20

Note: *These are Green Products which do not contain hazardous substances.*

3 Pin Assignment

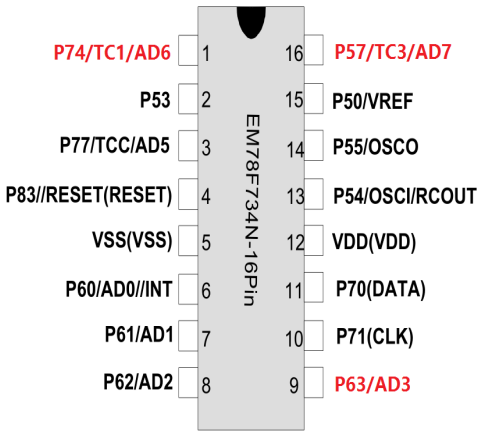


Figure 3-1 EM78F734ND16/SO16/SO16A/SS16

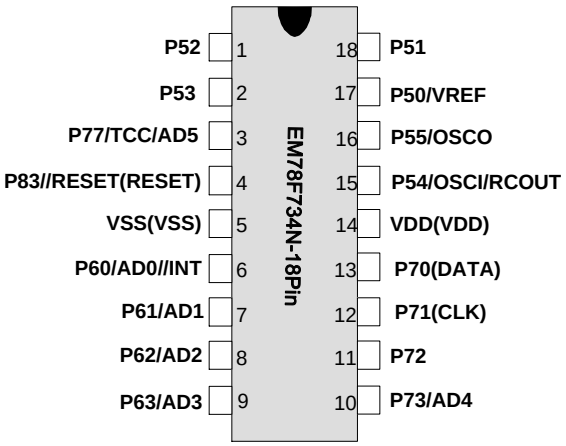


Figure 3-2 EM78F734ND18/SO18

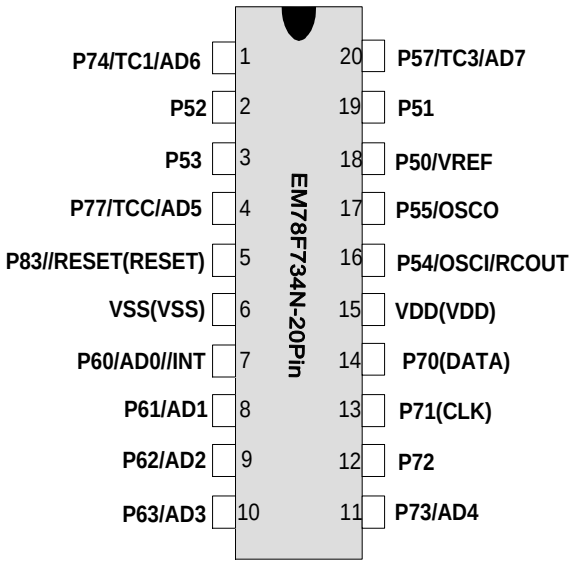


Figure 3-3 EM78F734ND20/SO20/SS20

4 Pin Description

Table 1 EM78F734N Pin Description

Legend: ***ST:*** *Schmitt Trigger input* ***AN:*** *analog pin*
CMOS: *CMOS output* ***XTAL:*** *Oscillation pin for crystal / resonator*

Name	Function	Input Type	Output Type	Description
P50/VREF	P50	ST	CMOS	Bidirectional I/O pin with programmable pull-down
	VREF	AN	–	ADC external voltage reference
P51	P51	ST	CMOS	Bidirectional I/O pin with programmable pull-down
P52	P52	ST	CMOS	Bidirectional I/O pin with programmable pull-down
P53	P53	ST	CMOS	Bidirectional I/O pin with programmable pull-down
P54/OSCI/RCOUT	P54	ST	CMOS	Bidirectional I/O pin
	OSCI	XTAL	–	External clock crystal resonator oscillator input pin
	RCOUT	–	CMOS	Clock output of internal RC oscillator Clock output of external RC oscillator (open-drain)
P55/OSCO	P55	ST	CMOS	Bidirectional I/O pin
	OSCO	–	XTAL	Clock output from crystal oscillator
P57/TC3/AD7	P57	ST	CMOS	Bidirectional I/O pin
	TC3	ST	–	Timer 3 input (Counter/Capture/Window) Timer 3 output (PDO/PWM/Buzzer)
	PDO	–	CMOS	Programmable divider output
	AD7	AN	–	ADC Input 7
P60/AD0//INT	P60	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	AD0	AN	–	ADC Input 0
	/INT	ST	–	External interrupt pin
P61/AD1	P61	ST	CMOS	Bidirectional I/O pin with programmable pull-down, pull-high, open-drain, and pin change wake-up
	AD1	AN	–	ADC Input 1

6 Functional Description

6.1 Operational Registers

6.1.1 R0 (Indirect Addressing Register)

R0 is not a physically implemented register. It is used as an indirect addressing pointer. Any instruction using R0 as a pointer actually accesses data pointed by the RAM Select Register (R4).

6.1.2 R1 (Timer Clock/Counter)

R1 is incremented by an external signal edge, which is defined by TE bit (CONT-4) through the TCC pin, or by the instruction cycle clock. It is writable and readable as any other registers. It is defined by resetting PSTE (CONT-3).

The prescaler is assigned to TCC, if the PSTE bit (CONT-3) is reset. The contents of the prescaler counter are cleared only when the TCC register is written with a value.

6.1.3 R2 (Program Counter) and Stack

Depending on the device type, R2 and hardware stack are 10-bit wide. The structure is depicted in Figure 6-1.

The configuration structure generates 4K×13 bits on-chip Flash ROM addresses to the relative programming instruction codes. One program page is 1024 words long.

R2 is set as all “0”s when under a reset condition.

“JMP” instruction allows direct loading of the lower 10 program counter bits. Thus, “JMP” allows PC to go to any location within a page (1K).

“CALL” instruction loads the lower 10 bits of the PC, and then PC+1 is pushed into the stack. Thus, the subroutine entry address can be located anywhere within a page.

“LJMP” instruction allows direct loading of the program counter bits (A0~A11). Thus, “LJMP” allows the PC to go to any location within 4K (2^{12}).

“LCALL” instruction loads the program counter bits (A0~A11), and PC+1 are pushed onto the stack. Thus, the subroutine entry address can be located anywhere within 4K (2^{12}).

“RET” (“RETL k”, “RETI”) instruction loads the program counter with the contents of the top-level stack.

“ADD R2, A” allows a relative address to be added to the current PC, and the ninth and above bits of the PC will increase progressively.

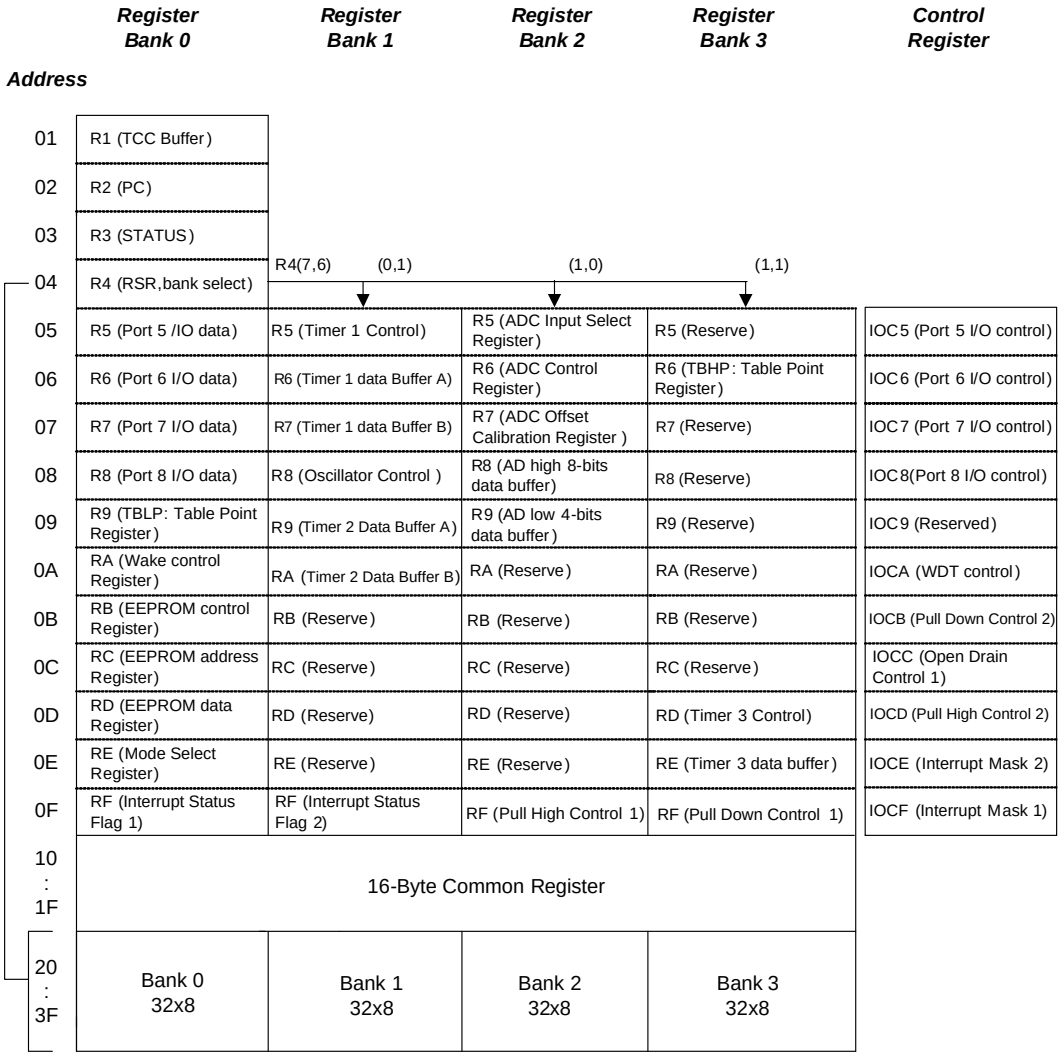


Figure 6-2 Data Memory Configuration

6.1.4 R3 (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	T	P	Z	DC	C

Bits 7 ~ 5: Not used, set to "**0**" at all time

Bit 4 (T): Time-out bit

Set to "**1**" with the "SLEP" and "WDTC" commands, or during power up and reset to "**0**" by WDT time-out.

Bit 3 (P): Power down bit

Set to "**1**" during power on or by a "WDTC" command and reset to "**0**" by a "SLEP" command.

Bit 2 (Z): Zero flag

Set to "**1**" if the result of an arithmetic or logic operation is zero.

Bit 1 (DC): Auxiliary carry flag

Bit 0 (C): Carry flag

6.1.5 R4 (RAM Select Register)

Bits 7 ~ 6: Used to select Bank 0 ~ Bank 3

Bits 5 ~ 0: Used to select registers (Address: 00~3F) in indirect addressing mode.

See the data memory configuration in Figure 6-2.

6.1.6 Bank 0 R5 ~ R8 (Port 5 ~ Port 8)

R5 ~ R7 are I/O registers.

6.1.7 Bank 0 R9 TBPTL (Low byte of Table Pointer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RBit 7	RBit 6	RBit 5	RBit 4	RBit 3	RBit 2	RBit 1	RBit 0

6.1.13 Bank 0 RF (Interrupt Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	ADIF	-	-	-	EXIF	ICIF	TCIF

Note: ***" 1 "*** *means with interrupt request* ***" 0 "*** *means no interrupt occurs*

Bit 7: Not used, set to "**0**" at all time

Bit 6 (ADIF): Interrupt flag for analog to digital conversion. Set when AD conversion is completed, reset by software.

Bits 5 ~ 3: Not used, set to "**0**" at all time

Bit 2 (EXIF): External interrupt flag. Set by a falling edge on /INT pin, reset by software.

Bit 1 (IC IF): Port 6 input status change interrupt flag. Set when Port 6 input changes,reset by software.

Bit 0 (TCIF): TCC overflow interrupt flag. Set when TCC overflows, reset by software.

Bank 0 RF can be cleared by instruction but cannot be set.

IOCF is the interrupt mask register.

NOTE

The result of reading Bank 0 RF is t"e "logic "ND" of Bank 0 RF and IOCF.

6.1.14 R10 ~ R3F

These are all 8-bit general-purpose registers.

6.1.15 Bank 1 R5 TC1CR (Timer 1 Control)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC1CAP	TC1S	TC1M	TC1ES	TC1MOD	TCK1CK2	TC1CK1	TC1CK0

Bit 7 (TC1CAP): Software capture control

0 : Software capture disable

1 : Software capture enable

Bit 6 (TC1S): Timer/Counter 1 start control

0 : Stop and clear the counter

1 : Start Timer/Counter 1

Bit 5 (TC1M): Timer/Counter 1 mode select

0 : Timer/Counter 1 mode

1 : Capture mode

Bit 4 (TC1ES): TC1 signal edge

0 : increment if the transition from low to high (rising edge) takes place on the TC1 pin.

1 : increment if the transition from high to low (falling edge) takes place on TC1 pin.

Bit 3 (TC1MOD): Timer Operation Mode Selection Bit

0: Two 8-bit timers

1: Timer 1 and 2 are cascaded as one 16-bit timer. The corresponding control register of 16-bit timer is from timer 1. TC1DA and TC2DA are low byte. TC1DB and TC2DB are high byte.

Bit 2 ~ Bit 0 (TC1CK2 ~ TC1CK0): Timer/Counter 1 clock source select

TC1CK2	TC1CK1	TC1CK0	Clock Source	Resolution 8 MHz	Max. time 8 MHz	Resolution 16kHz	Max. time 16kHz
			Normal	F_C=8M	F_C=8M	F_C=16K	F_C=16K
0	0	0	$F_C/2^{23}$	1.05s	19.1hr	145hr	9544hr
0	0	1	$F_C/2^{13}$	1.024ms	67.11s	512ms	33554.432s
0	1	0	$F_C/2^8$	32μs	2.097s	16ms	1048.576s
0	1	1	$F_C/2^3$	1μs	65.536ms	0.5ms	32768ms
1	0	0	$F_C/2^2$	0.5μs	32.768ms	0.25ms	16384ms
1	0	1	$F_C/2$	0.25μs	16.384ms	125μs	8192ms
1	1	0	F_C	125ns	8.192ms	0.0625ms	4096ms
1	1	1	External clock (TC1 pin)	-	-	-	-

Bits 1 ~ 0: Not used, set to "**0**" at all time.

6.1.18 Bank 1 R8 OSCR (Oscillator Control)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RCM1	RCM0	–	–	–	–	–	–

Bit 7 and Bit 6 (RCM1, RCM0): IRC mode select bits

Writer Trim IRC	Bank1 R8<7,6>		Frequency
	RCM1	RCM0	
4 MHz	**0**	**0**	4 MHz
	0	**1**	1 MHz
	1	**0**	8 MHz
	1	**1**	455kHz
1 MHz	**0**	**0**	4 MHz
	0	**1**	1 MHz
	1	**0**	8 MHz
	1	**1**	455kHz
8 MHz	**0**	**0**	4 MHz
	0	**1**	1 MHz
	1	**0**	8 MHz
	1	**1**	455kHz
455kHz	**0**	**0**	4 MHz
	0	**1**	1 MHz
	1	**0**	8 MHz
	1	**1**	455kHz

NOTE

- *Bank 1 R8<7, 6 > of the initialized values are kept the same as Word 1<3,2>.*
- *After A Frequency switches to B Frequency, EM78F734N needs to hold some stable time on B frequency*
  ***Ex:** Writer trim IRC 4 MHz → Bank 1 R8<7,6> set to "10" → holds 3 µs → EM78F734N works on 8 MHz ± 10%*

Code Option Word 1 COBS=0**:**

The R8<7, 6 > of the initialized values will remain the same as Word 1<3, 2>.

The R8<7, 6 > cannot change frequency.

Code Option Word 1 COBS=1:

The R8<7, 6 > of the initialized values will remain the same Word as 1<3, 2>.

The R8<7, 6> can change when user wants to work on other IRC frequency.

6.1.19 Bank 1 R9 TC2DA (Timer 2 Data Buffer A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC2DA7	TC2DA6	TC2DA5	TC2DA4	TC2DA3	TC2DA2	TC2DA1	TC2DA0

Bits 7~0 (TC2DA7~ TC2DA0): Data buffer of 8-bit Timer/Counter 2 cascade with Timer/Counter 1 at TC1MOD set to "1"

6.1.20 Bank 1 RA TC2DB (Timer 2 Data Buffer B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC2DB7	TC2DB6	TC2DB5	TC2DB4	TC2DB3	TC2DB2	TC2DB1	TC2DB0

Bit 7 ~ Bit 0 (TC2DB7 ~ TC2DB0): Data buffer of 8-bit Timer/Counter 2 cascade with Timer/Counter 1 at TC1MOD set to "1" ..

6.1.21 Bank 1 RB ~RE

These are reserved registers.

6.1.22 Bank 1 RF (Interrupt Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	TCIF3	–	TCIF1	-	-	-

***Note: " 1 "** means with interrupt request **" 0 "** means no interrupt occurs*

Bits 7~6: Not used, set to "**0**" at all time

Bit 5 (TCIF3): 8-bit Timer/Counter 3 interrupt flag. The Interrupt flag is cleared by software.

Bit 4: Not used, set to "**0**" at all time

Bit 3 (TCIF1): 8-bit Timer/Counter 1 interrupt flag. The Interrupt flag is cleared by software.

Bits 2~0: Not used, set to "0" at all time

Bank 1 RF can be cleared by instruction but cannot be set.

IOCE is the interrupt mask register.

NOTE
The result of reading Bank 1 RF is t"e "Logic "ND" of Bank 1 RF and IOCE.

6.1.28 Bank 2 RA ~ RE

These are reserved registers.

6.1.29 Bank 2 RF (Pull-high Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	/PH73	/PH72	/PH71	/PH70

Bits 7 ~ 4: Not used, set to "**0**" at all time.

Bit 3 (/PH73): Control bit used to enable pull-high of the P73 pin

0 : Enable internal pull-high

1 : Disable internal pull-high

Bit 2 (/PH72): Control bit used to enable pull-high of the P72 pin.

Bit 1 (/PH71): Control bit used to enable pull-high of the P71 pin.

Bit 0 (/PH70): Control bit used to enable pull-high of the P70 pin.

The RF Register is both readable and writable.

6.1.30 Bank 3 R5

Reserved Register

6.1.31 Bank 3 R6 TBPTH (High Byte of Table Pointer Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MLB	0	0	0	RBit 11	RBit 10	RBit 9	RBit 8

Bit 7 (MLB): Take MSB or LSB at machine code.

Bits 6 ~ 4: Not used. Set to "**0**" at all time.

Bits 3 ~ 0: Table Pointer Address Bits 11~8.

6.1.32 Bank 3 R7~RC

Reserved Registers

6.1.33 Bank 3 RD TC3CR (Timer 3 Control)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC3FF1	TC3FF0	TC3S	TC3CK2	TC3CK1	TC3CK0	TC3M1	TC3M0

Bit 7 ~ Bit 6 (TC3FF1 ~ TC3FF0): Timer/Counter 3 flip-flop control

TC3FF1	TC3FF0	Operating Mode
0	0	Clear
0	1	Toggle
1	0	Set
1	1	Reserved

Bit 5 (TC3S): Timer/Counter 3 start control

0 : Stop and clear the counter

1 : Start Timer/Counter 3

Bit 4 ~ Bit 2 (TC3CK2 ~ TC3CK0): Timer/Counter 3 Clock Source select

TC3CK2	TC3CK1	TC3CK0	Clock Source	Resolution	Max. Time
			Normal	Fc=8M	Fc=8M
0	0	0	$Fc/2^{11}$	250 µs	64 ms
0	0	1	$Fc/2^{7}$	16 µs	4 ms
0	1	0	$Fc/2^{5}$	4 µs	1 ms
0	1	1	$Fc/2^{3}$	1 µs	255 µs
1	0	0	$Fc/2^{2}$	500 ns	127.5 µs
1	0	1	$Fc/2^{1}$	250 ns	63.8 µs
1	1	0	Fc	125 ns	31.9 µs
1	1	1	External clock (TC3 pin)	-	-

Bit 1 ~ Bit 0 (TC3M1 ~ TC3M0): Timer/Counter 3 operating mode select

TC3M1	TC3M0	Operating Mode
0	0	Timer/Counter
0	1	Reserved
1	0	Programmable Divider output
1	1	Pulse Width Modulation output

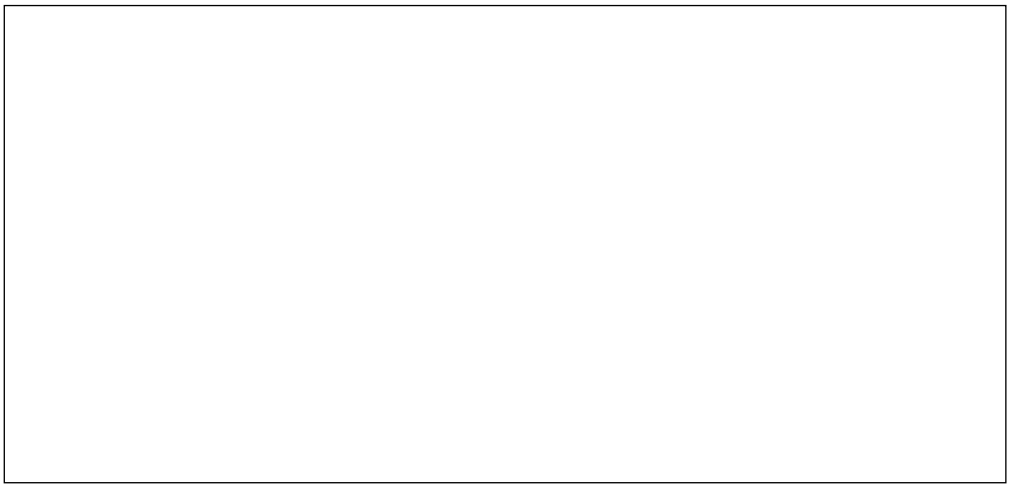


Figure 6-6 Timer / Counter 3 Configuration

In Timer mode, counting up is performed using internal clock (rising edge trigger). When the contents of the up-counter match the TCR3, then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared.

In Counter mode, counting up is performed using external clock input pin (TC3 pin). When the contents of the up-counter match the TCR3, then interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared.

In Programmable Divider Output (PDO) mode, counting up is performed using the internal clock. The contents of TCR3 are compared with the contents of the up-counter. The F/F output is toggled and the counter is cleared each time a match is found. The F/F output is inverted and output to /PDO pin. This mode can generate 50% duty pulse output. The F/F can be initialized by the program and it is initialized to "**0**" during reset. A TC3 interrupt is generated each time the /PDO output is toggled.

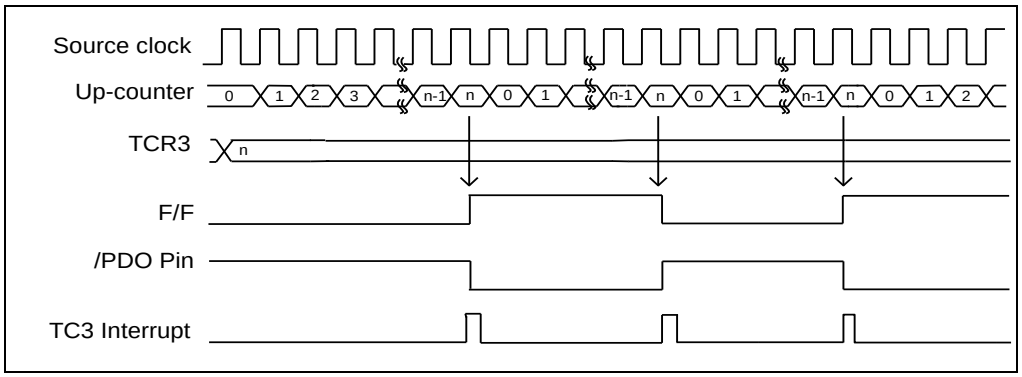


Figure 6-7 PDO Mode Timing Chart

In Pulse Width Modulation (PWM) Output mode, counting up is performed using internal clock. The contents of TCR3 are compared with the contents of the up-counter and TCR3 should be greater than 1(including 1) . The F/F is toggled when a match is found. The counter continues counting, the F/F is toggled again when the counter overflows, after which the counter is cleared. The F/F output is inverted and output to /PWM pin. A TC3 interrupt is generated each time an overflow occurs. TCR3 is configured as a 2-stage shift register and, during output, will not switch until one output cycle is completed even if TCR3 is overwritten. Therefore, the output can be changed continuously. Also, the first time, TRC3 is shifted by setting TC3S to "**1**" after data is loaded to TCR3.

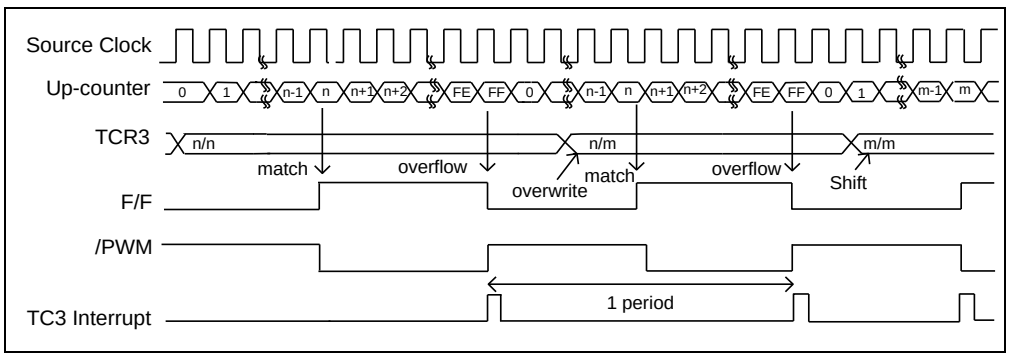


Figure 6-8 PWM Mode Timing Chart

6.1.34 Bank 3 RE TC3D (Timer 3 Data Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TC3D7	TC3D6	TC3D5	TC3D4	TC3D3	TC3D2	TC3D1	TC3D0

Bit 7 ~ Bit 0 (TC3D7 ~ TC3D0): Data Buffer of 8-bit Timer/Counter 3

6.1.35 Bank 3 RF (Pull-down Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	-	/PD73	/PD72	/PD71	/PD70

Bit 7~ Bit 4: Not used, set to "**0**" at all time

Bit 3 (/PD73): Control bit used to enable the P73 pull-down pin

0 : Enable internal pull-down

1 : Disable internal pull-down

Bit 2 (/PD72): Control bit used to enable the P72 pull-down pin

Bit 1 (/PD71): Control bit used to enable the P71 pull-down pin

Bit 0 (/PD70): Control bit used to enable the P70 pull-down pin

The RF Register is both readable and writable.

6.2 Special Function Registers

6.2.1 A (Accumulator)

Internal data transfer operation, or instruction operand holding usually involves the temporary storage function of the Accumulator, which is not an addressable register.

6.2.2 CONT (Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE	/INT	TS	TE	PSTE	PST2	PST1	PST0

Bit 7 (INTE): INT signal edge

0 : interrupt occurs at the rising edge of the INT pin

1 : interrupt occurs at the falling edge of the INT pin

Bit 6 (/INT): Interrupt Enable flag

0 : masked by DISI or hardware interrupt

1 : enabled by ENI/RETI instructions

Bit 5 (TS): TCC signal source

0 : internal instruction cycle clock

1 : transition on the TCC pin

Bit 3 (TCIE1): Interrupt enable bit

0: Disable TCIF1 interrupt

1: Enable TCIF1 interrupt

Bits 2~0: Not used, set to "**0**" at all time

6.2.10 IOCF (Interrupt Mask Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	ADIE	–	–	–	EXIE	ICIE	TCIE

Bit 7: Not used, set to "**0**" at all time

Bit 6 (ADIE): ADIF interrupt enable bit

0 : Disable ADIF interrupt

1 : Enable ADIF interrupt

When the ADC Complete is used to enter an interrupt vector or enter the next instruction, the ADIE bit must be set to "Enable".

Bits 5 ~ 3: Not used, set to "0" at all time

Bit 2 (EXIE): EXIF interrupt enable bit

0 : Disable EXIF interrupt

1 : Enable EXIF interrupt

Perform the following steps from the EXINT, First set EXIE, and then set the EIS. EXINT internal comparison value default is "0". Then set the rising edge and the INT pin to high, since doing EXINT setting will cause immediate trigger signal and generate an interrupt.

Bit 1 (ICIE): ICIF interrupt enable bit

0 : Disable ICIF interrupt

1 : Enable ICIF interrupt

Bit 0 (TCIE): TCIF interrupt enable bit

0 : Disable TCIF interrupt

1 : Enable TCIF interrupt

Individual interrupt is enabled by setting its associated control bit in the IOCF to "1".

Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. The IOCF register is both readable and writable.

6.3 TCC/WDT and Prescaler

There are two 8-bit counters available as prescalers for the TCC and WDT respectively. The PST0~PST2 bits of the CONT register are used to determine the ratio of the prescaler of TCC. Likewise, the PSW0~PSW2 bits of the IOCA register are used to determine the WDT prescaler. The prescaler counter will be cleared by the instructions each time they are written into TCC. The WDT and prescaler will be cleared by the "WDTC" and "SLEP" instructions. Figure 6-9 depicts the circuit diagram of TCC/WDT.

R1 (TCC) is an 8-bit timer/counter. The clock source of TCC can be the internal clock or the external signal input (edge selectable from the TCC pin). If TCC signal source is from the internal clock, TCC will be incremented by 1 at Fc clock (without prescaler). As illustrated in Figure 6-9, selection of Fc depends on the bank 0 RE.6 <TIMERSC>. If TCC signal source is from external clock input, TCC will be incremented by 1 at every falling edge or rising edge of the TCC pin. TCC pin input time length (kept in High or low level) must be greater than 1CLK. The TCC will stop running when sleep mode occurs.

The watchdog timer is a free running on-chip RC oscillator. The WDT will keep on running even after the oscillator driver has been turned off (i.e. in sleep mode). During normal operation or sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled at any time during normal mode by software programming. Refer to WDTE bit of IOCA register. With no prescaler, the WDT time-out period is approximately 16.5 ms[1] (one oscillator start-up timer period).

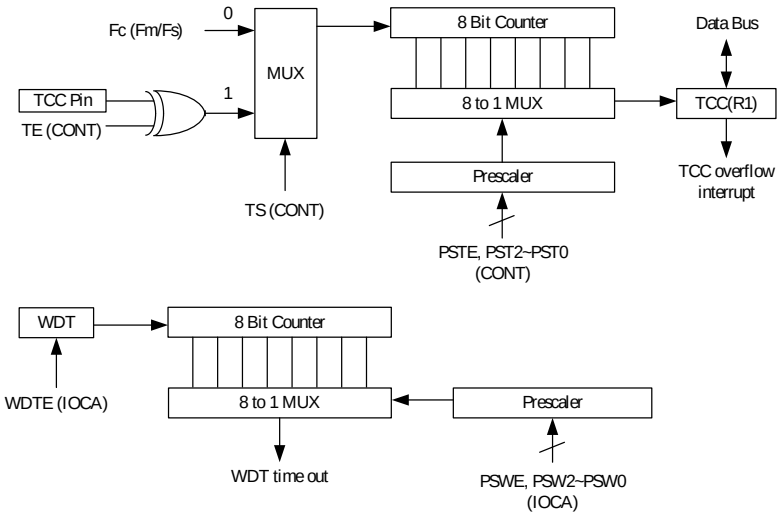
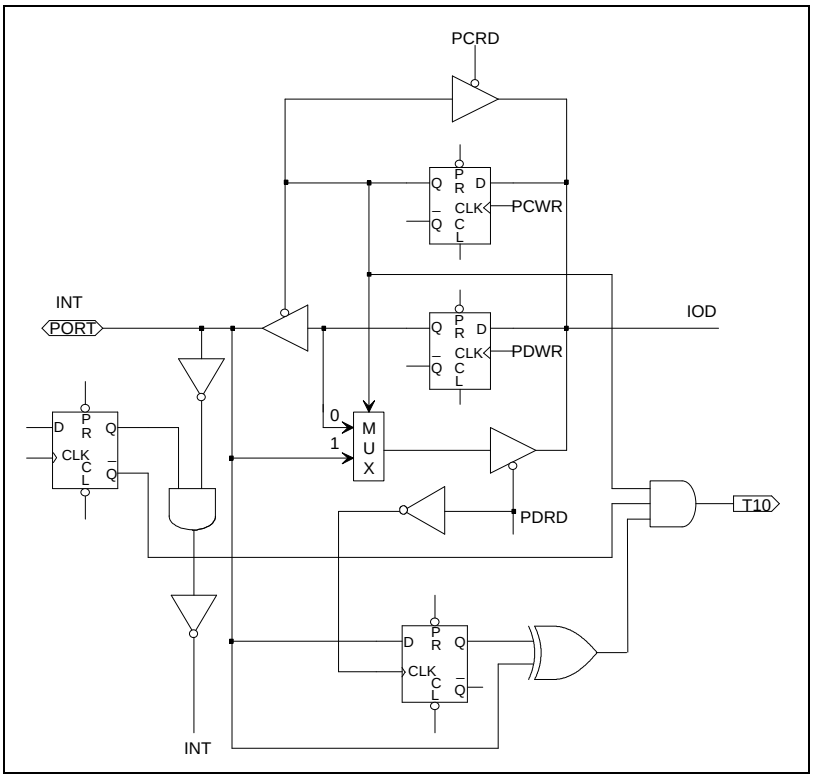


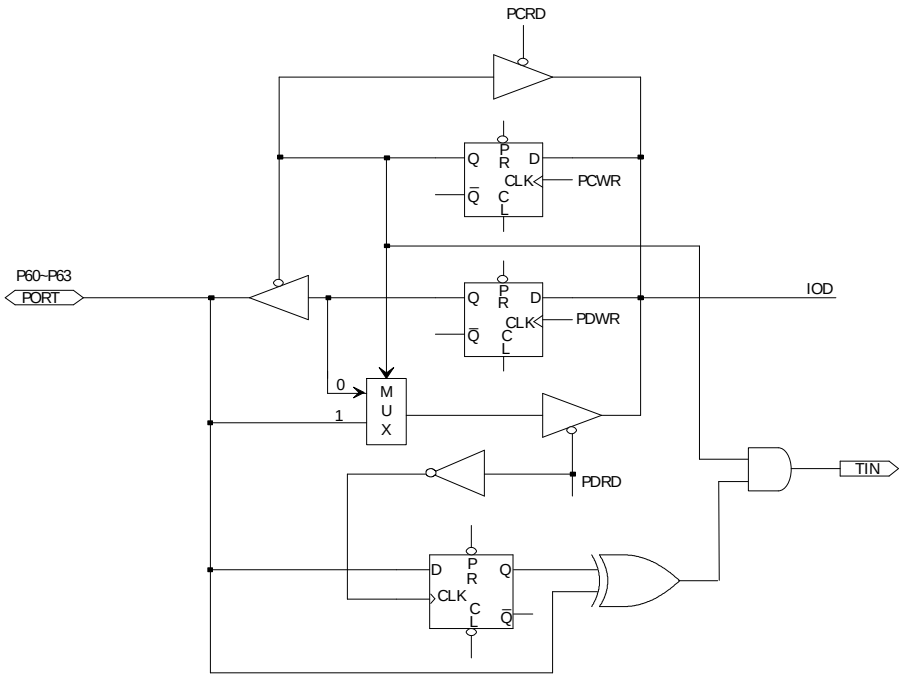
Figure 6-9 TCC and WDT Block Diagram

[1] VDD=5V, WDT time-out period = 16.5ms ± 5% VDD=3V
WDT time-out period = 16.5ms ± 5%.



Note: *Pull-high (down) and Open-drain are not shown in the figure.*

Figure 6-11 (a) I/O Port and I/O Control Register Circuit for P60 (INT)



Note: *Pull-high (down) and Open-drain are not shown in the figure.*

Figure 6-11 (b) I/O Port and I/O Control Register Circuit for P61~P63, P83

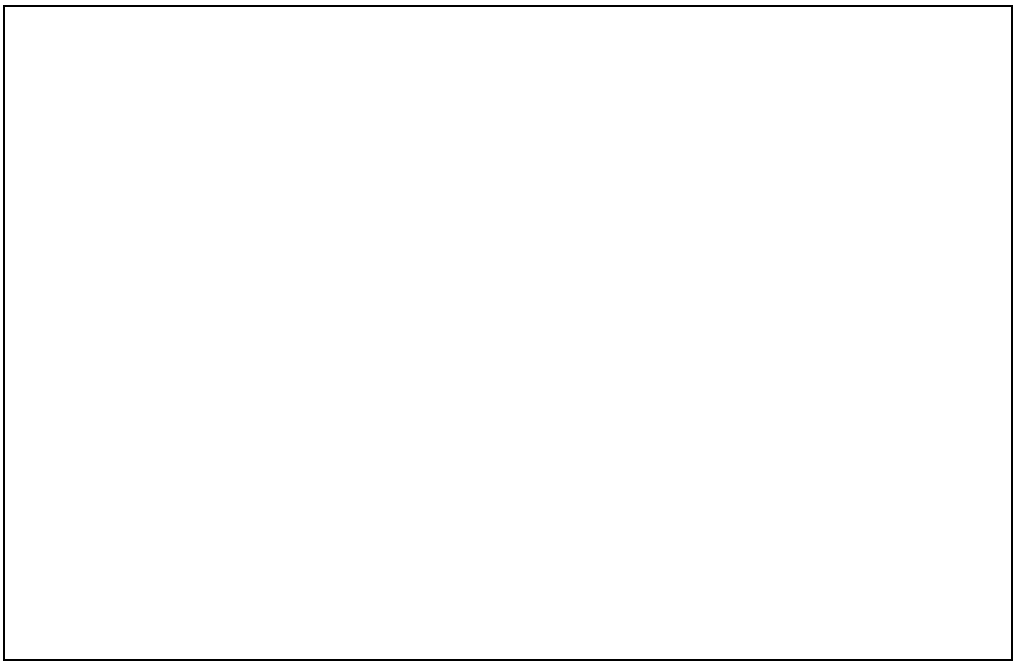


Figure 6-12 Block Diagram of I/O Port 6 with Input Change Interrupt/Wake-up

Table 6-1 Usage of Port 6 Input Change Wake-up/Interrupt Function

Usage of Port 6 Input Status Changed Wake-up/Interrupt	
(I) Wake-up Input Status Change **(a) Before Sleep** 1. Disable WDT[2] (use this very carefully) 2. Read I/O Port 6 (MOV R6,R6) 3 a. Enable interrupt (Set IOCF=1), after wake-up if "ENI" switch to interrupt vector (006H), if "DISI" excute next instruction 3 b. Disable interrupt (Set IOCF=1). Always execute next instruction 4. Enable wake-up bit (Set RA=6) 5. Execute "SLEP" instruction **(b) After Wake-up** 1. If "NI" → Interrupt Vector (006H) 2. If "DSI" → Next instruction	**(II) Interrupt Input Status Change** 1. Read I/O Port 6 (MOV R6,R6) 2. Execute "NI" 3. Enable interrupt (Set IOCF=1) 4. If Port 6 change (Interrupt) → Interrupt Vector (006H)

[2] *Software disables WDT (watchdog timer) but hardware must be enabled before applying Port 6 Change Wake-up function (Code Option Register Word 0 Bit 6 (ENWDTB) is set to "1").*
[3] *Vdd = 5V, set up time period = 16.5ms ± 5%*
Vdd = 3V, set up time period = 16.5ms ± 5%

Addr	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x05	P5 (Bank 0)	Bit Name	P57	-	P55	P54	P53	P52	P51	P50
		Power-on	1	0	1	1	1	1	1	1
		/RESET and WDT	1	0	1	1	1	1	1	1
		Wake-up from Pin Change	P	0	P	P	P	P	P	P
0x06	P6 (Bank 0)	Bit Name	-	-	-	-	P63	P62	P61	P60
		Power-on	0	0	0	0	1	1	1	1
		/RESET and WDT	0	0	0	0	1	1	1	1
		Wake-up from Pin Change	0	0	0	0	P	P	P	P
0x07	P7 (Bank 0)	Bit Name	P77	-	-	P74	P73	P72	P71	P70
		Power-on	1	0	0	1	1	1	1	1
		/RESET and WDT	1	0	0	1	1	1	1	1
		Wake-up from Pin Change	P	0	0	P	P	P	P	P
0x08	P8 (Bank 0)	Bit Name	-	-	-	-	P83	-	-	-
		Power-on	0	0	0	0	1	0	0	0
		/RESET and WDT	0	0	0	0	1	0	0	0
		Wake-up from Pin Change	0	0	0	0	P	0	0	0
0X09	R9 (Bank 0)	Bit Name	RBit7	RBit6	RBit5	RBit4	RBit3	RBit2	RBit1	RBit0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x0A	RA (Bank 0)	Bit Name	-	ICWE	ADWE	EXWE	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	P	P	P	0	0	0	0
0X0B	RB (ECR) (Bank 0)	Bit Name	RD	WR	EEWE	EEDF	EEPC	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	P	P	P	P	P	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	0	0	0
0X0C	RC (Bank 0)	Bit Name	-	EE_A6	EE_A5	EE_A4	EE_A3	EE_A2	EE_A1	EE_A0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	P	P	P	P	P	P	P
		Wake-up from Pin Change	0	P	P	P	P	P	P	P
0X0D	RD (Bank 0)	Bit Name	EE_D7	EE_D6	EE_D5	EE_D4	EE_D3	EE_D2	EE_D1	EE_D0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X0E	RE (Bank 0)	Bit Name	-	TIMERSC	CPUS	IDLE	-	-	-	-
		Power-on	0	1	1	1	0	0	0	0
		/RESET and WDT	0	1	1	1	0	0	0	0
		Wake-up from Pin Change	0	P	P	P	0	0	0	0

Addr	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0F	RF (ISR) (Bank 0)	Bit Name	-	ADIF	-	-	-	EXIF	ICIF	TCIF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	P	0	0	0	P	P	P
0x5	R5 (Bank 1)	Bit Name	TC1AP	TC1S	TC1M	TC1ES	TC1MOD	TCK1CK2	TC1CK1	TC1CK0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x6	R6 (Bank 1)	Bit Name	TC1DA7	TC1DA6	TC1DA5	TC1DA4	TC1DA3	TC1DA2	TC1DA1	TC1DA0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0X7	R7 (Bank 1)	Bit Name	TC1DB7	TC1DB6	TC1DB5	TC1DB4	TC1DB3	TC1DB2	TC1DB1	TC1DB0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x8	R8 (Bank 1)	Bit Name	RCM1	RCM0	-	-	-	-	-	-
		Power-on	Option RCM1	Option RCM0	0	0	0	0	0	0
		/RESET and WDT	Option RCM1	Option RCM0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	0	0	0	0	0	0
0x9	R9 (Bank 1)	Bit Name	TC2DA7	TC2DA6	TC2DA5	TC2DA4	TC2DA3	TC2DA2	TC2DA1	TC2DA0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0XA	RA (Bank 1)	Bit Name	TC2DB7	TC2DB6	TC2DB5	TC2DB4	TC2DB3	TC2DB2	TC2DB1	TC2DB0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0XF	RF (Bank 1)	Bit Name	-	-	TCIF3	-	TCIF1	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	P	0	P	0	0	0
0x05	R5 (Bank 2)	Bit Name	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P

Addr	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x06	R6 (Bank 2)	Bit Name	VREFS	CKR1	CKR0	ADRUN	ADPD	ADIS2	ADIS1	ADIS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x7	R7 (Bank 2)	Bit Name	-	-	-	-	-	PDE	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	0	0	0	P	0	0
0x8	R8 (Bank 2)	Bit Name	ADD11	ADD10	ADD9	ADD8	ADD7	ADD6	ADD5	ADD4
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x9	R9 (Bank 2)	Bit Name	-	-	IRVS1	IRVS0	ADD3	ADD2	ADD1	ADD0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	P	P	P	P	P	P
0x0F	RF (Bank 2)	Bit Name	-	-	-	-	/PH73	/PH72	/PH71	/PH70
		Power-On	0	0	0	0	1	1	1	1
		/RESET and WDT	0	0	0	0	1	1	1	1
		Wake-up from Pin Change	0	0	0	0	P	P	P	P
0X06	R6 (Bank 3)	Bit Name	MLB	-	-	-	RBit 11	RBit 10	RBit 9	RBit 8
		Power-On	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	0	0	0	P	P	P	P
0XD	RD (Bank 3)	Bit Name	TC3FF1	TC3FF0	TC3S	TC3CK2	TC3CK1	TC3CK0	TC3M1	TC3M0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0XE	RE (Bank 3)	Bit Name	TC3D7	TC3D6	TC3D5	TC3D4	TC3D3	TC3D2	TC3D1	TC3D0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0XF	RF (Bank 3)	Bit Name	-	-	-	-	/PD73	/PD72	/PD71	/PD70
		Power-on	0	0	0	0	1	1	1	1
		/RESET and WDT	0	0	0	0	1	1	1	1
		Wake-up from Pin Change	0	0	0	0	P	P	P	P

The flag (except ICIF bit) in the Interrupt Status Register (RF) is set regardless of the status of its mask bit or the execution of ENI. The RETI instruction ends the interrupt routine and enables the global interrupt (the execution of ENI).

The external interrupt is equipped with an on-chip digital noise rejection circuit (input pulse less than **8 system clock time** is eliminated as noise)**.** When an interrupt (Falling edge) is generated by the External interrupt (when enabled), the next instruction will be fetched from Address 003H.

Before the interrupt subroutine is executed, the contents of ACC and the R3 and R4 register will be saved by hardware. If another interrupt occurred, the ACC, R3 and R4 will be replaced by the new interrupt. After the interrupt service routine is finished, ACC, R3 and R4 will be pushed back.

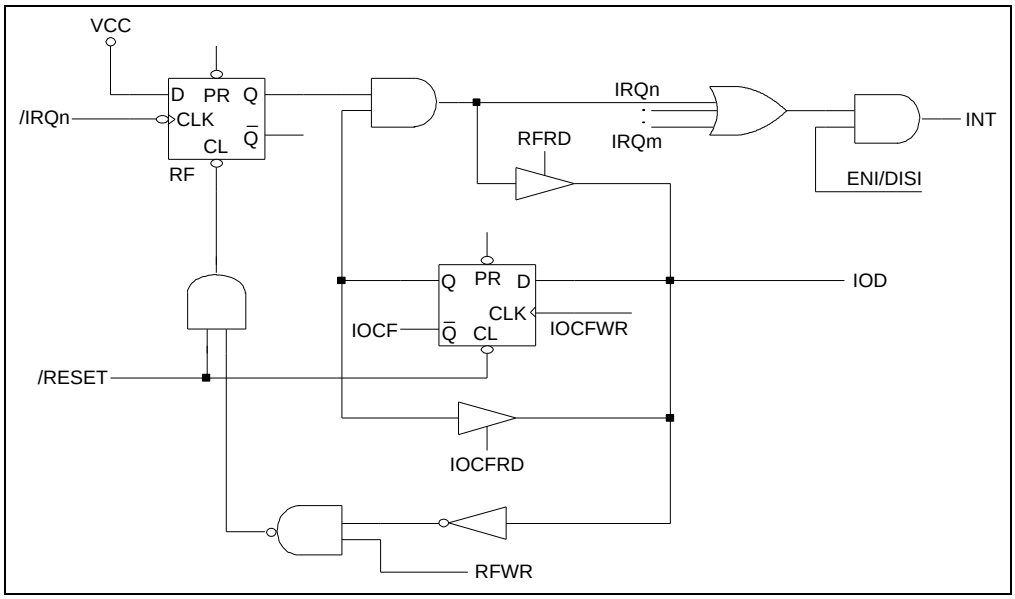


Figure 6-14 Interrupt Input Circuit

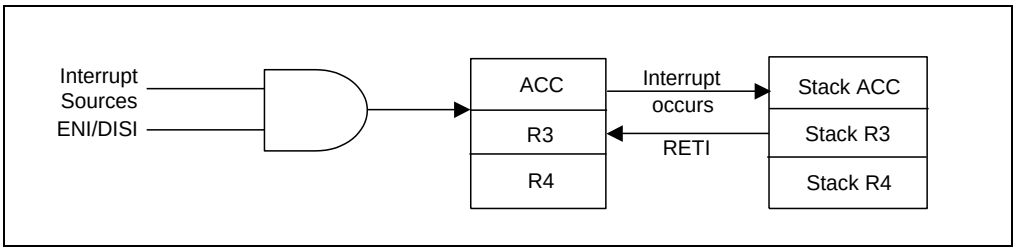


Figure 6-15 Interrupt Back-up Diagram

6.8.7 A/D Conversion Time

CKR0 and CKR1 select the conversion time (Tct), in terms of instruction cycles. This allows the MCU to run at the maximum frequency without sacrificing the accuracy of A/D conversion. For the EM78F734N, the conversion time per bit is 1μs. The table below shows the relationship between Tct and the maximum operating frequencies.

■ **Tct vs. Maximum Operation Frequency**

CKR0: CKR1	Operation Mode	Max. Operating Frequency	Max. Conversion Rate Per Bit	Max. Conversion Rate (12bit)
00	Fosc/4	4 MHz	1 MHz (1 μs)	(12+8)*1μs=20μs (50kHz)
01	Fosc	1 MHz	1 MHz (1μs)	(12+4)*1μs=16μs(62.5kHz)
10	Fosc/16	8 MHz	0.5 MHz (2 μs)	(12+12)*2μs=48μs (20.8kHz)
11	Fosc/2	1 MHz	0.5 MHz (2 μs)	(12+4)*2μs=32μs (31.25kHz)

NOTE

- *The pin that is not used as analog input can be used as regular input or output pin.*
- *During conversion, do not perform output instruction to maintain precision for all of the pins.*

6.8.8 A/D Operation during Sleep Mode

In order to obtain a more accurate ADC value and reduced power consumption, the A/D conversion remains operational during sleep mode. As the SLEP instruction is executed, all the MCU operations will stop except for the Oscillator, TCC, TC1, TC3, and A/D conversion.

The AD Conversion is considered completed when:

1 ADRUN Bit of R6 Register is cleared to "**0**".

2 Wake-up from A/D Conversion remains in operation during Sleep Mode.

The result is fed to the ADDATA, ADOC when the conversion is completed. If the ADWE is enabled, the device will wake up. Otherwise, the A/D conversion will be shut off, no matter what the status of the ADPD bit is.

■ Timer Mode

In Timer mode, counting up is performed using the internal clock (rising edge trigger). When the contents of the up-counter matched with TCR3, interrupt is generated and the counter is cleared. Counting up resumes after the counter is cleared.

■ Counter Mode

In Counter mode, counting up is performed using the external clock input pin (TC3 pin). When the contents of the up-counter matched with TCR3, interrupt is then generated and the counter is cleared. Counting up resumes after the counter is cleared.

■ Programmable Divider Output (PDO) Mode

In Programmable Divider Output (PDO) mode, counting up is performed using the internal clock. The contents of TCR3 are compared with the contents of the up-counter. The F/F output is toggled and the counter is cleared each time a match is found. The F/F output is inverted and output to /PDO pin. This mode can generate 50% duty pulse output. **The F/F can be initialized by program and it is initialized to "0" during reset.** A TC3 interrupt is generated each time the /PDO output is toggled.

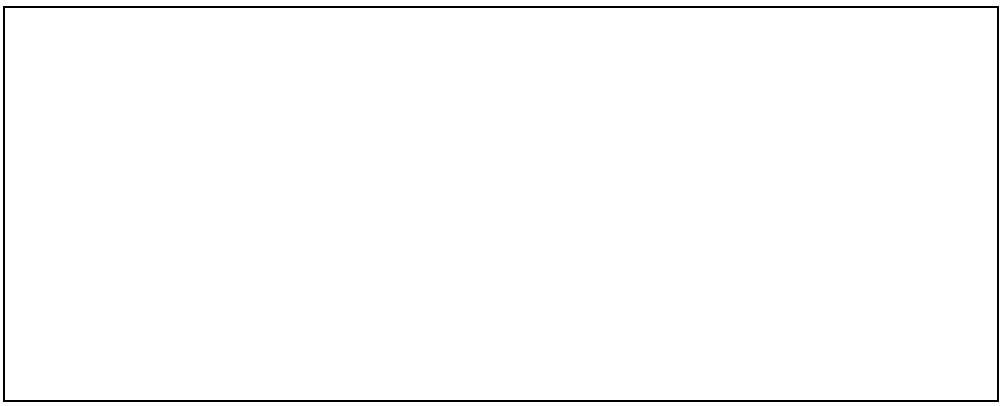


Figure 6-20 PDO Mode Timing Diagram

■ Pulse Width Modulation (PWM) Output Mode

In Pulse Width Modulation (PWM) Output mode**,** counting up is performed using the internal clock. The contents of TCR3 are compared with the contents of the up-counter. The F/F is toggled when a match is found. While the counter is counting, the F/F is toggled again when the counter overflows, then the counter is cleared. The F/F output is inverted and output to the /PWM pin. A TC3 interrupt is generated each time an overflow occurs. **TCR3 is configured as a 2-stage shift register and during output, will not switch until one output cycle is completed even if TCR3 is overwritten.** Hence, the output can be changed continuously. Also, on the first time, TRC3 is shifted by setting TC3S to "**1**" after data is loaded to TCR3.

The following table provides the recommended values of C1 and C2. Since each resonator has its own attributes, you should refer to its specification for appropriate values of C1 and C2. A serial resistor RS, may be necessary for AT strip cut crystal or low frequency mode.

■ **Capacitor Selection Guide for Crystal Oscillator or Ceramic Resonator**

Oscillator Type	Frequency Mode	Frequency	C1(pF)	C2(pF)
Ceramic Resonators	LXT1 (100K~1 MHz)	100kHz	60pF	60pF
		200kHz	60pF	60pF
		455kHz	40pF	40pF
		1 MHz	30pF	30pF
	XT (1M~6 MHz)	1.0 MHz	30pF	30pF
		2.0 MHz	30pF	30pF
		4.0 MHz	20pF	20pF
Crystal Oscillator	LXT1 (100K~1 MHz)	100kHz	60pF	60pF
		200kHz	60pF	60pF
		455kHz	40pF	40pF
		1 MHz	30pF	30pF
	XT (1~6 MHz)	1.0 MHz	30pF	30pF
		2.0 MHz	30pF	30pF
		4.0 MHz	20pF	20pF
		6.0 MHz	30pF	30pF
	HXT1 (6~12 MHz)	6.0 MHz	30pF	30pF
		8.0 MHz	20pF	20pF
		12.0 MHz	30pF	30pF
	HXT2 (12~20 MHz)	12.0 MHz	30pF	30pF
		16.0 MHz	20pF	20pF

6.14 Power-on Considerations

Any microcontroller is not guaranteed to start to operate properly before the power supply stays has stabilized. The EM78F734N has an on-chip Power-on Voltage Detector (POVD) with a detecting level of 2.0V. It will work well if Vdd can rise quickly enough (50ms or less). In many critical applications, however, extra devices are still required to assist in solving power-up problems.

6.15 External Power-on Reset Circuit

The circuit shown in Figure 6-24 uses an external RC to generate a reset pulse. The pulse width (time constant) should be kept long enough for Vdd to reached minimum operation voltage. This circuit is used when the power supply has slow rise time. Because the current leakage from the /RESET pin is ± 5μA, it is recommended that R should not be greater than 40K. In this way, the /RESET pin voltage is held below 0.2V. The diode (D) functions as a short circuit at the moment of power down.

The capacitor C will discharge rapidly and fully. Rin, the current-limited resistor, will prevent high current or ESD (electrostatic discharge) from flowing to pin /RESET.

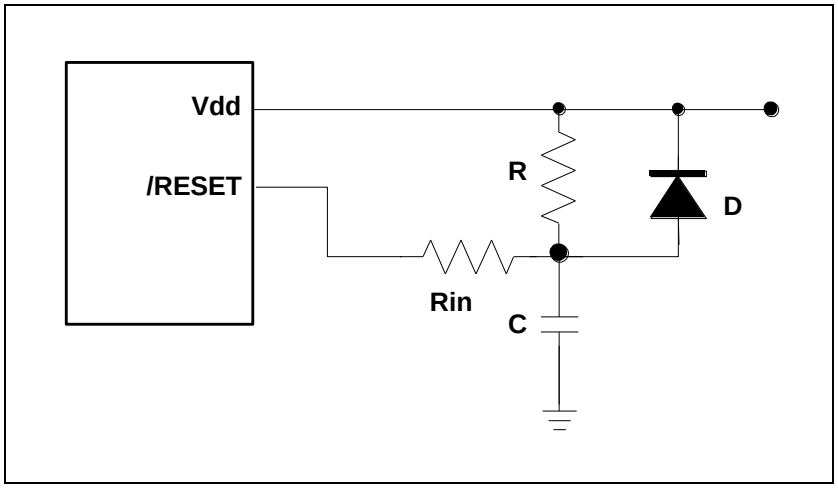


Figure 6-24 External Power-up Reset Circuit

6.16 Residue-Voltage Protection

When battery is replaced, device power (Vdd) is taken off but residue-voltage remains. The residue-voltage may trip below Vdd minimum, but not to zero. This condition may cause a poor power-on reset. Figure 6-25 and Figure 6-26 show how to build a residue-voltage protection circuits.

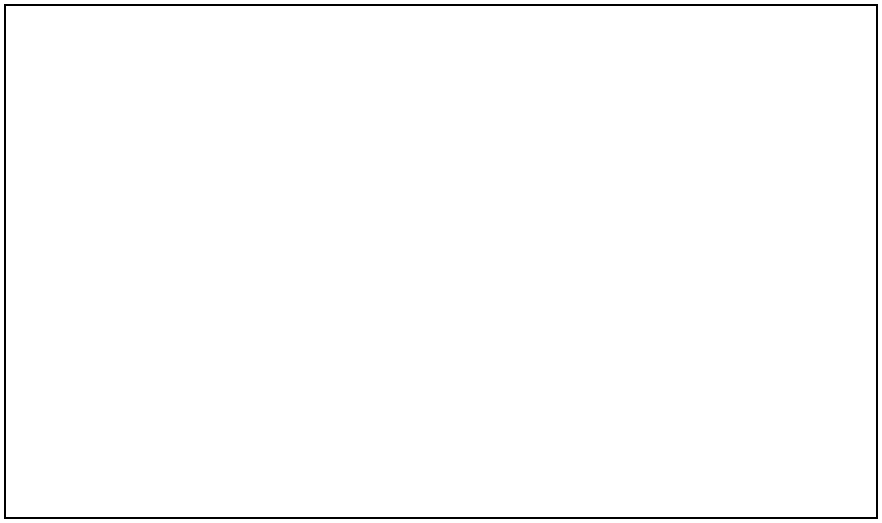


Figure 6-25 Circuit 1 for the Residue Voltage Protection

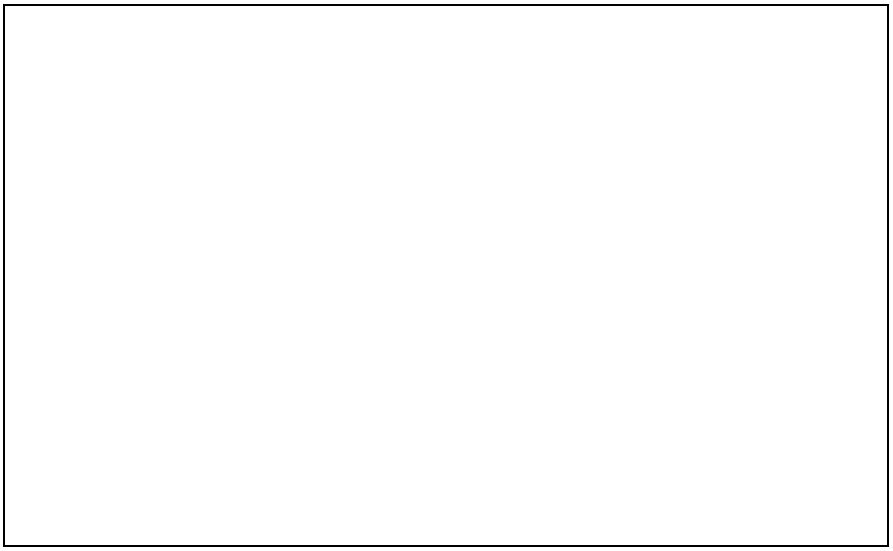


Figure 6-26 Circuit 2 for the Residue Voltage Protection

6.17 Instruction Set

Each instruction in the instruction set is a 13-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of two oscillator periods), unless the program counter is changed by instru“tion "MO” R“,A", "AD” R2,A", or by instructions of arithmetic or logic operation on R2 “e.g. "SU” R“,A", "BS(C” R“,6", "”LR R2", ····). In this case, the execution takes two instruction cycles.

(300)If for some reasons, the specification of the instruction cycle is not suitable for certain applications, try modifying the instruction as fol“(A)” "“MP","”"C“LL"” "“ET","”"R“TL","”"RETI" commands are executed with one instruction cycle, the conditional “kip”("“BS"” "“BC”, “JZ"” "“ZA"” "“JZ","”"DJZA") commands which were tested to be true, are executed within two instruction cycles. The instructions that are written to the program counter also take two instruction cycles.

In addition, the instruction set has the following features:

(1) Every bit of any register can be set, cleared, or tested directly.

(2) The I/O register can be regarded as general register. That is, the same instruction can operate on the I/O register.

■ Instruction Set Table:

The following symbols are used in the following table:

*"**R**" Register designator that specifies which one of the registers (including operation and general purpose registers) is to be utilized by the instruction.*

*"**b**" Bit field designator that selects the value for the bit located in the register R and which affects the operation.*

*"**K**" 8 or 10-bit constant or literal value*

Mnemonic	Operation	Status Affected
NOP	No Operation	None
DAA	Decimal Adjust A	C
CONTW	A → CONT	None
SLEP	0 → WDT, Stop oscillator	T, P
WDTC	0 → WDT	T, P
IOW R	A → IOCR	None[1]
ENI	Enable Interrupt	None
DISI	Disable Interrupt	None
RET	[Top of Stack] → PC	None
RETI	[Top of Stack] → PC, Enable Interrupt	None
CONTR	CONT → A	None
IOR R	IOCR → A	None[1]
MOV R,A	A → R	None
CLRA	0 → A	Z
CLR R	0 → R	Z
SUB A,R	R-A → A	Z, C, DC
SUB R,A	R-A → R	Z, C, DC
DECA R	R-1 → A	Z
DEC R	R-1 → R	Z
OR A,R	A ∨ R → A	Z
OR R,A	A ∨ R → R	Z
AND A,R	A & R → A	Z
AND R,A	A & R → R	Z
XOR A,R	A ⊕ R → A	Z
XOR R,A	A ⊕ R → R	Z
ADD A,R	A + R → A	Z, C, DC
ADD R,A	A + R → R	Z, C, DC
MOV A,R	R → A	Z
MOV R,R	R → R	Z
COMA R	/R → A	Z
COM R	/R → R	Z
INCA R	R+1 → A	Z
INC R	R+1 → R	Z

[1] *This instruction is applicable to IOC5~IOC7, IOCA ~ IOCF only.*

8 Absolute Maximum Ratings

■ **EM78F734N**

Items	Rating		
Temperature under bias	-40°C	to	85°C
Storage temperature	-65°C	to	150°C
Working voltage	2.2	to	5.5V
Working frequency	DC	to	20 MHz*
Input voltage	Vss-0.3V	to	Vdd+0.5V
Output voltage	Vss-0.3V	to	Vdd+0.5V

Note: **These parameters are theoretical values and have not been tested.*

9 DC Electrical Characteristics

VDD=5.0V, VSS=0V, Ta=25°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Fxt	Crystal: VDD to 3V	Two cycles with two clocks	DC	-	4	MHz
	Crystal: VDD to 5V		DC	-	20	MHz
	IRC: VDD to 5 V	4 MHz, 455kHz, 1 MHz,,8 MHz	F±30%	F	F±30%	Hz
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	-	-	±1	μA
VIHRC	Input High Threshold Voltage (Schmitt Trigger)	OSCI in RC mode	3.9	4	4.1	V
VILRC	Input Low Threshold Voltage (Schmitt Trigger)	OSCI in RC mode	1.7	1.8	1.9	V
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	-1	0	1	μA
VIH1	Input High Voltage (Schmitt trigge)	Ports 5, 6, 7, 8	-	0.7VDD (2.8V)	-	V
VIL1	Input Low Voltage (Schmitt trigger)	Ports 5, 6, 7, 8	-	0.3VDD (2.2V)	-	V
VIHT1	Input High Threshold Voltage (Schmitt Trigger)	/RESET	-	0.7VDD	-	V
VILT1	Input Low Threshold Voltage (Schmitt trigger)	/RESET	-	0.3VDD	-	V
VIHT2	Input High Threshold Voltage (Schmitt Trigger)	TCC, INT	-	0.7VDD	-	V
VILT2	Input Low Threshold Voltage (Schmitt Trigger)	TCC, INT	-	0.3VDD	-	V
VIHX1	Clock Input High Voltage	OSCI in crystal mode	2.9	3.0	3.1	V
VILX1	Clock Input Low Voltage	OSCI in crystal mode	1.7	1.8	1.9	V

Note: ** The parameters are theoretical and have not been tested or verified.*

** Data in the Minimum, Typical, Maximum ("Min.", "T"p.", "Max.") column are based on hypothetical results at 25℃. These data are for design guidance only.*

10 AC Electrical Characteristics

EM78F734N, 0 ≤ Ta ≤ 70°C, VDD=5V, VSS=0V

-40 ≤ Ta ≤ 85°C, VDD=5V, VSS=0V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Dclk	Input CLK duty cycle	–	45	50	55	%
Tins	Instruction cycle time ”C”KS="0")	Crystal type	100	–	DC	ns
		RC type	500	–	DC	ns
Ttcc	TCC input period	–	(Tins+20)/N*	–	–	ns
Tdrh	Device reset hold time	–	11.8	16.8	21.8	ms
Trst	/RESET pulse width	Ta = 25°C	2000	–	–	ns
Twdt	Watchdog timer period	Ta = 25°C	11.8	16.8	21.8	ms
Tset	Input pin setup time	–	–	0	–	ns
Thold	Input pin hold time	–	–	20	–	ns
Tdelay	Output pin delay time	Cload=20pF	–	50	–	ns

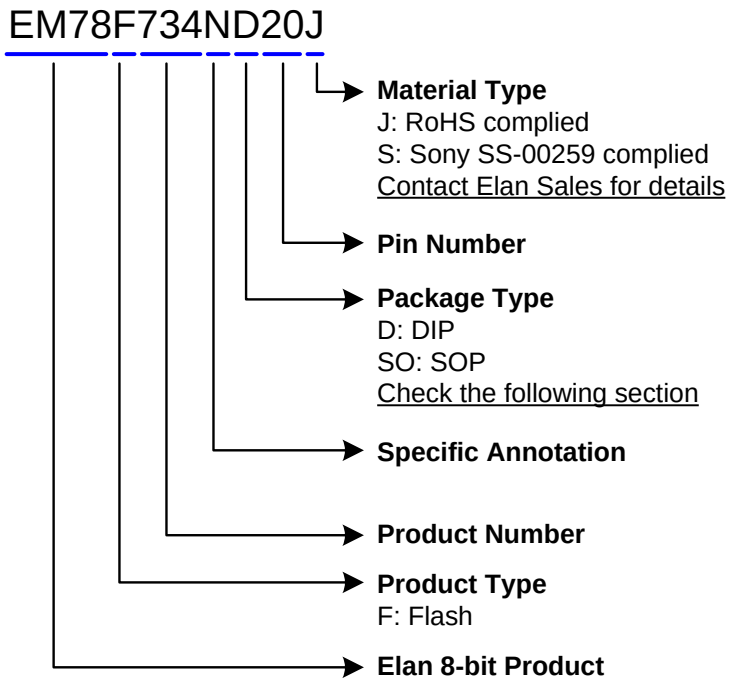
Note: These parameters are theoretical values and have not been tested. Such parameters are for design reference only.

Data in the Minimum, Typical, Maximum (“Min.”, “Typ.”, ”Max.”) columns are based on characterization results at 25°C.

* N = selected prescaler ratio

APPENDIX

A Ordering and Manufacturing Information



For example:

EM78F734NSO20S

is EM78F734N with Flash program memory, product,
in 20-pin SOP 300mil package with Sony SS-00259 complied

IC Mark

C.2 EM78F734NSO16 300mil

Figure B-2 EM78F734N 16-Pin SOP Package Type

C.3 EM78F734NSO16A 150mil

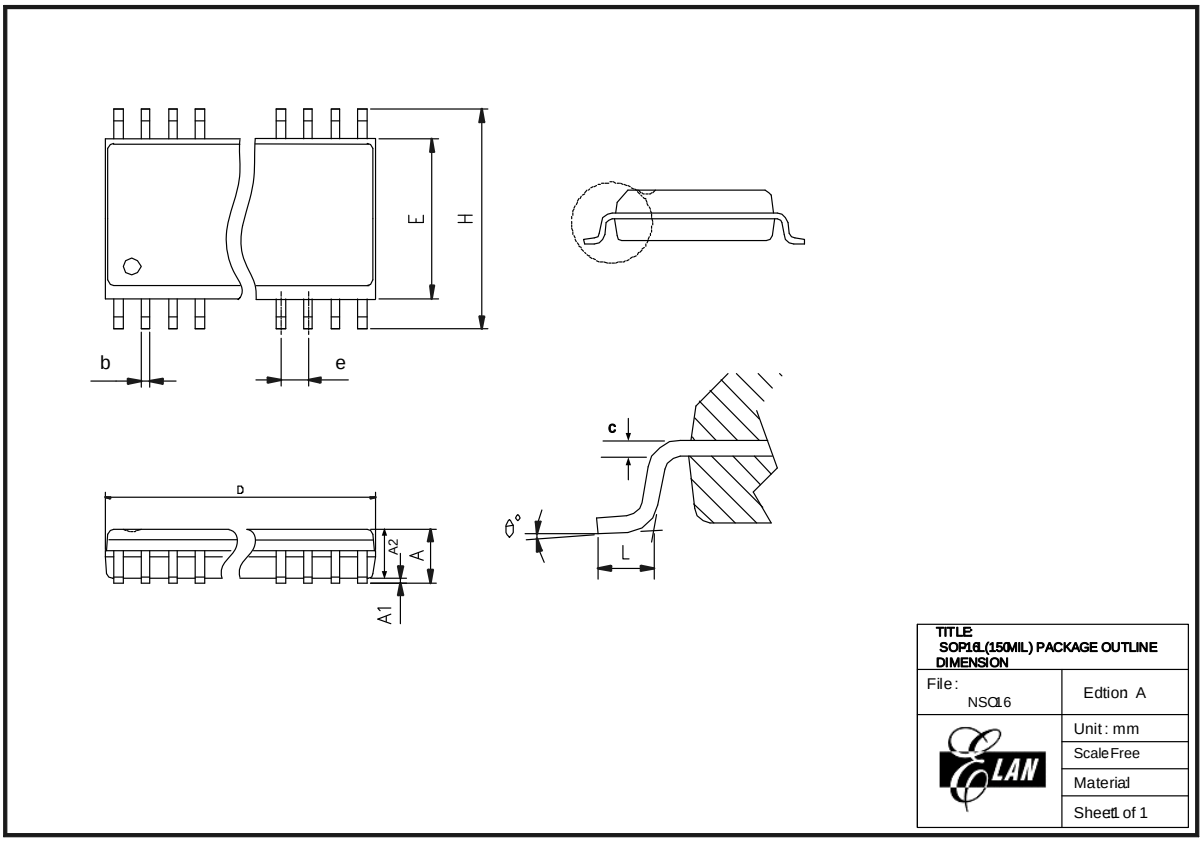
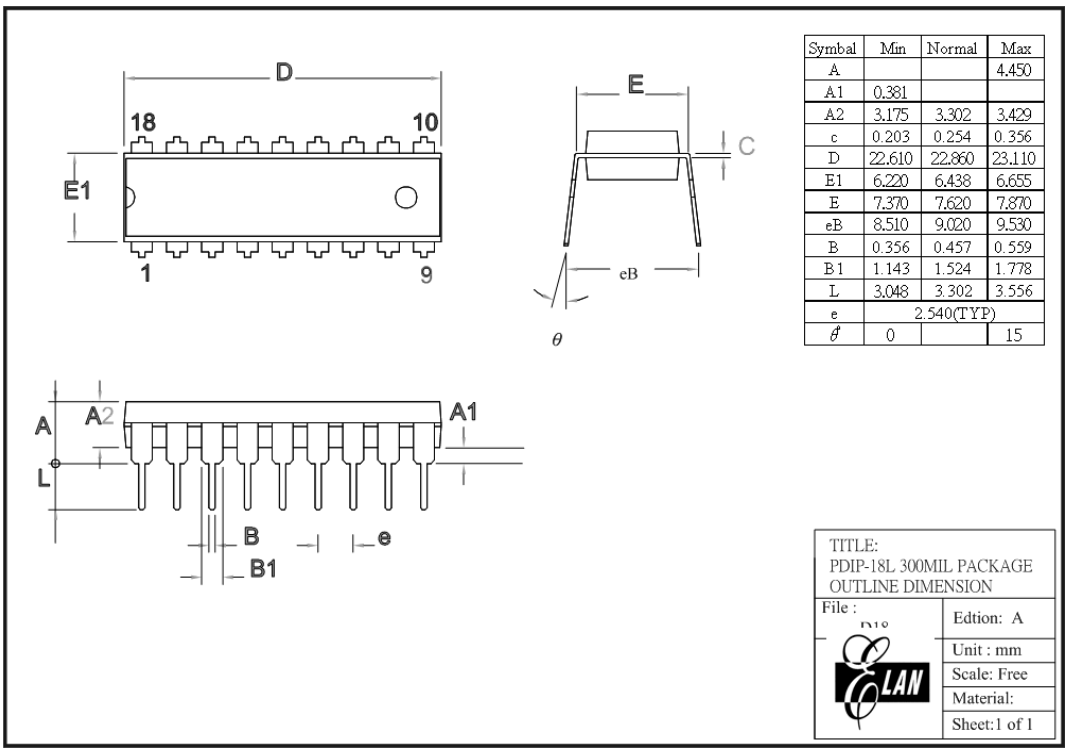


Figure B-3 EM78F734N 16-Pin SOP Package Type

C.5 EM78F734ND18 300mil



Symbal	Min	Normal	Max
A			4.450
A1	0.381		
A2	3.175	3.302	3.429
c	0.203	0.254	0.356
D	22.610	22.860	23.110
E1	6.220	6.438	6.655
E	7.370	7.620	7.870
eB	8.510	9.020	9.530
B	0.356	0.457	0.559
B1	1.143	1.524	1.778
L	3.048	3.302	3.556
e	2.540(TYP)		
θ°	0		15

Figure B-5 EM78F734N 18-Pin PDIP Package Type

C.7 EM78F734ND20 300mil

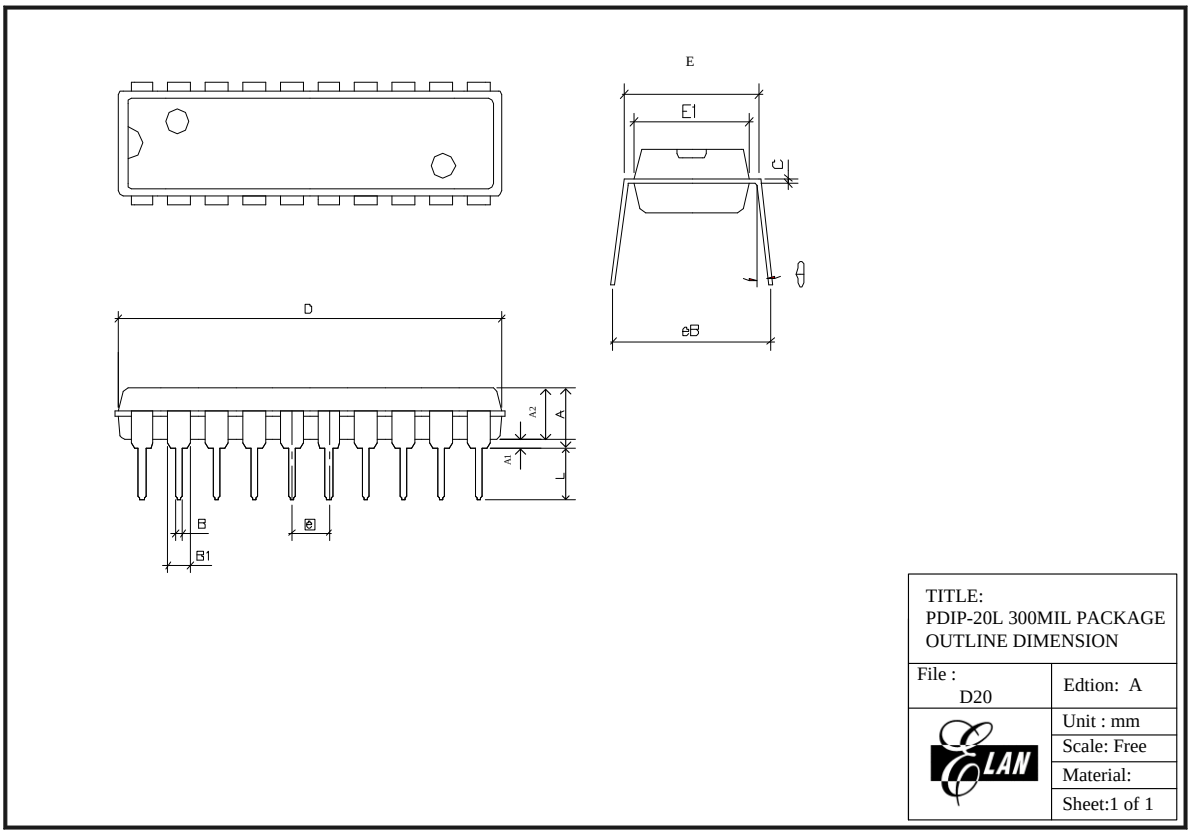


Figure B-7 EM78F734N 20-Pin PDIP Package Type

C.9 EM78F734NSS20 209mil

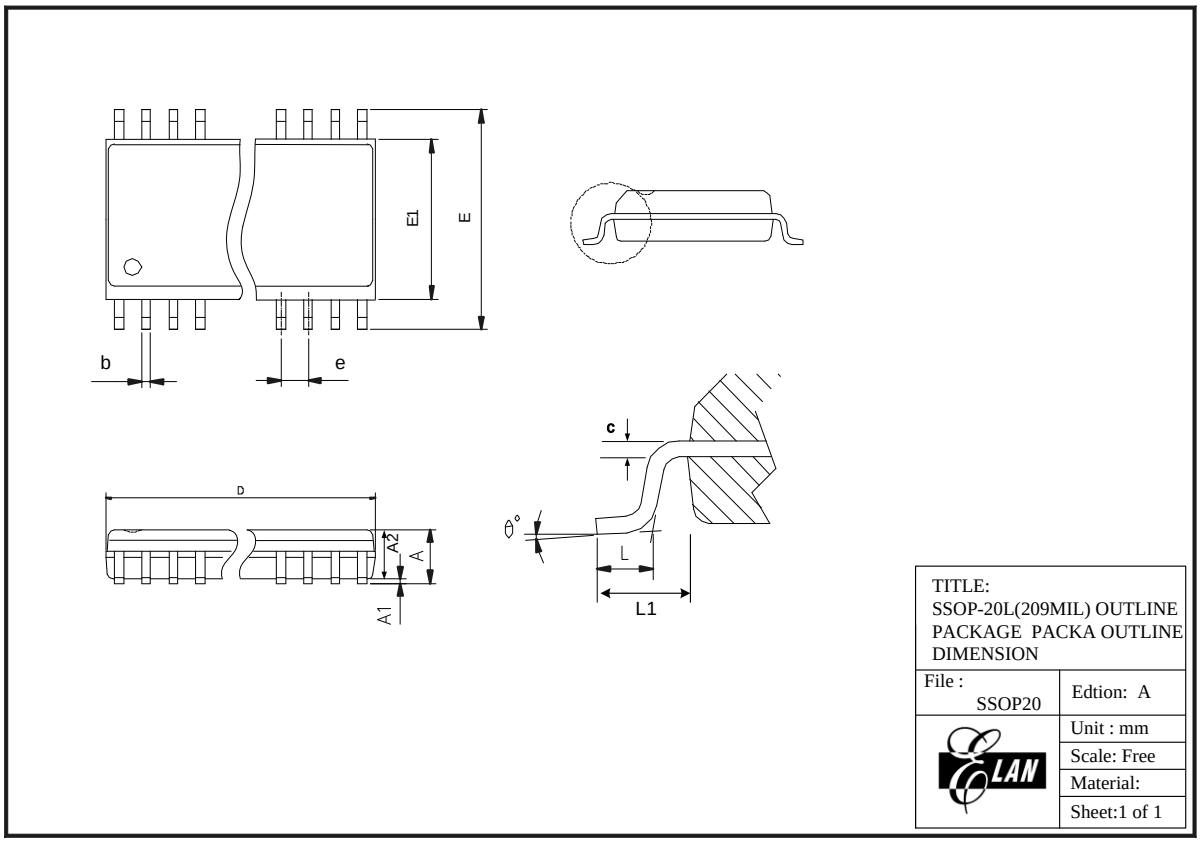


Figure B-9 EM78F734N 20-Pin SSOP Package Type